

**REMARKS**

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated July 28, 2005 has been received and its contents carefully reviewed.

By this Response, claims 1, 16 and 30 have been amended, and claims 13-14 and 27-28 have been cancelled without prejudice or disclaimer of the subject matter recited therein. No new matter has been added. Claims 1-10, 15-24 and 29-36 are pending in the application. Reconsideration and withdrawal of the rejections in view of the above amendments and the following remarks are respectfully requested.

In the Office Action, claims 1, 7-10, 13-16, 24 and 27-29 are rejected under 35 U.S.C. § 130(a) as being unpatentable over Applicant's Related Art (ARA) in view of U.S. Patent No. 6,507,382, issued to Sakamoto et al. (hereafter "Sakamoto") and U.S. Patent No. 5,581,382, issued to Kim (hereafter "Kim"). Applicants respectfully traverse the rejection because neither ARA, Sakamoto nor Kim, analyzed alone or in any combination, teaches or suggests the combined features recited in the claims of the present application. For example, ARA, Sakamoto and Kim fail to teach or suggest an in-plane switching liquid crystal display device that includes, among other features, "a gate insulation layer on the first substrate;... a first passivation layer on the gate insulation layer;... a second passivation layer on the first passivation layer... wherein the gate insulation layer and the first passivation layer include a plurality of common line contact holes, wherein the first passivation layer and the second passivation layer include a drain contact hole exposing a drain electrode, wherein one of the plurality of pixel electrodes is electrically connected to the drain electrode through the drain contact hole" as recited in amended, independent claim 1 of the present application.

ARA, Sakamoto and Kim also fail to teach or suggest a method of fabricating an array substrate for an in-plane switching liquid crystal device including, among other features, "forming a gate insulation layer on the substrate... forming a first passivation layer on the gate insulation layer... forming a second passivation layer on the first passivation layer... wherein forming the gate insulation layer and the first passivation layer includes forming a plurality of common line contact holes, wherein a drain contact hole that exposes a drain electrode is formed

in the first and second passivation layers, wherein one of the plurality of pixel electrodes is formed to electrically connect to the drain electrode through the contact hole” as recited in amended, independent claim 16 of the present application.

The Office Action concedes that ARA fails to teach all the features recited in the claims of the present application. To remedy the deficient teachings of ARA, the Office Action relies upon the teachings of Sakamoto and Kim. However, Applicants respectfully submit neither ARA, Sakamoto nor Kim teach or suggest at least the above features of claims 1 and 16. Thus, no combination of ARA, Sakamoto and Kim would provide the combined features recited in independent claims 1 and 16. Accordingly, claim 1 and its dependent claims 7-10 and 15, and independent claim 16 and its dependent claims 24 and 29 are allowable over any combination of ARA, Sakamoto and Kim. Reconsideration and withdrawal of the rejection are respectfully requested.

In the Office Action, claims 2-3 and 17-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ARA, Sakamoto and Kim, and further in view of U.S. Patent No. 6,356,328, issued to Shin et al. (hereafter “Shin”). Claims 4 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ARA in view of Sakamoto and Kim and further in view of U.S. Patent No. 6,163,355, issued to Chang et al. (hereafter “Chang”). And, claims 5-6 and 21-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ARA, Sakamoto and Kim, and further in view of U.S. Patent No. 6,414,729, issued to Akiyama et al. (hereafter “Akiyama”). Applicants respectfully traverse the rejections because neither ARA, Sakamoto, Kim, Shin, Chang, nor Akiyama, analyzed alone or in any combination, teaches or suggests the combined features recited in the claims of the present application. Specifically, ARA, Sakamoto, Kim, Shin, Chang and Akiyama fail to teach or suggest an in-plane switching liquid crystal display device that includes, among other features, “a gate insulation layer on the first substrate... a first passivation layer on the gate insulation layer... a second passivation layer on the first passivation layer... wherein the gate insulation layer and the first passivation layer include a plurality of common line contact holes, wherein the first passivation layer and the second passivation layer include a drain contact hole exposing a drain electrode, wherein one of the plurality of pixel electrodes is electrically connected to the drain electrode through the drain

contact hole” as recited in amended, independent claim 1 of the present application, from which claims 2-6 depend.

Further ARA, Sakamoto, Kim, Shin, Chang and Akiyama fail to teach or suggest a method of fabricating an array substrate for an in-plane switching liquid crystal device including, among other features, “forming a gate insulation layer on the substrate... forming a first passivation layer on the gate insulation layer... forming a second passivation layer on the first passivation layer... wherein forming the gate insulation layer and the first passivation layer includes forming a plurality of common line contact holes, wherein a drain contact hole that exposes a drain electrode is formed in the first and second passivation layers, wherein one of the plurality of pixel electrodes is formed to electrically connect to the drain electrode through the contact hole” as recited in amended, independent claim 16 of the present application, from which claims 17-23 depend.

Shin discloses “a technique of a liquid crystal display (LCD) with a counter electrode and a pixel electrode capable of minimizing an area on which liquid crystal molecules do not operate” (col. 1, lines 4-7). Chang discloses a manufacturing method for an IPS array of a TFT liquid crystal display to help resolve light leakage problems and reduce the resistance on the data line of an IPS LCD (see, col. 1, lines 8-10 and col. 2, lines 27-29). And, Akiyama discloses a LCD having “a shield electrode disposed below the lowest pixel electrode” (Abstract). However, Shin, Chang and Akiyama fail to provide teachings that would motivate one of ordinary skill in the art to modify the teachings of ARA, Sakamoto and Kim to provide all the combined features recited in claims 1 and 16 of the present application. Accordingly, claims 2-6 and 17-23, by virtue of their dependence from claims 1 and 16, respectively, are allowable over any combination of ARA, Sakamoto, Kim, Shin, Chang and Akiyama. Reconsideration and withdrawal of the rejections of claims 2-6 and 17-23 are respectfully requested.

In the Office Action, claims 30 and 31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ARA, Sakamoto and Kim, and further in view of U.S. Patent No. 6,300,995, issued to Wakagi et al. (hereafter “Wakagi”). Claims 32 and 33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ARA, Sakamoto, Kim and Wakagi and further in view of Shin. Claim 34 is rejected under 35 U.S.C. § 103(a) as being unpatentable over APA in view of

Sakamoto, Kim and Wakagi and further in view of Chang. And, claims 35 and 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ARA, Sakamoto and Wakagi and further in view of Akiyama. Applicants respectfully traverse the rejections because neither ARA, Sakamoto, Kim, Wakagi, Shin, Chang and Akiyama, analyzed alone or in any combination, teaches or suggests the combined features recited in the claims of the present application. In particular, ARA, Sakamoto, Kim, Wakagi, Shin, Chang and Akiyama fail to teach or suggest an in-plane switching liquid crystal display device that includes, “a first insulation layer over the gate lines,... a second insulation layer over the data lines and the common line; a plurality of first contact holes through the first and second insulation layers over the common line... a third insulation layer on the common electrodes and the second insulation layer... a second contact hole through the second and third insulation layers over a drain electrode of the thin film transistor; a plurality of pixel electrodes on the third insulation layer, wherein one of the plurality of pixel electrodes is electrically connected to the drain electrode through the second contact hole” as recited in amended, independent claim 30 of the present application.

Wakagi discloses a LCD device “to reduce losses in the driving voltage applied to the liquid crystal by providing an active matrix substrate in which degradation of the metal electrode is prevented” (col. 2, lines 7-10). However, Applicants respectfully submit Wakagi fails to provide teachings that would motivate one of ordinary skill in the art to modify the teachings of any combination of ARA, Sakamoto, Kim, Shin, Chang and Akiyama to provide an in-plane switching liquid crystal display device having the combined features recited in independent claim 30 of the present application.

Because no combination of ARA, Sakamoto, Kim, Wakagi, Shin, Chang and Akiyama teaches the above features of claim 30, claim 30 and its dependent claims 31-36 are allowable over any combination of ARA, Sakamoto, Kim, Wakagi, Shin, Chang and Akiyama. Reconsideration and withdrawal of the rejections are respectfully requested.

Applicants believe the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to

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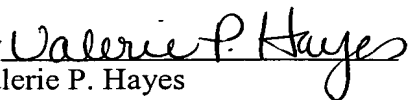
Docket No.: 8733.464.00

discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

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